SPECIFICATION AMENDMENTS

Please amend paragraph [**0024**] as follows.

[**0024**] FIG. 2 illustrates a portion of a host channel adapter (HCA) 60 referred to as a direct memory access (DMA) packet engine 65 used in the example embodiments of the present invention. It should be emphasized that the DMA packet engine 65 only makes up a small portion of either the HCA 60, TCA 90 or switch 80 or any other device that serves to transfer packets of information from one device to another. The DMA packet engine 65 communicates indirectly to the memory controller 50, shown in FIG. 1, through the in-bound multiplexer (IBM) bus 300 in which control information may be passed back and forth between HCA 60 and memory controller 50. IBM write data 290 may be utilized to write data to DRAM 40 through memory controller 50 from HCA 60. In turn, IBM fixed data 280 may be used to receive data from memory controller 50, shown in FIG. 1. The DMA packet engine 65 transmits and receives data to a switch 80 or TCA 90, shown in FIG. 1, via serial interface block (SIB) transmit bus 260 and a SIB receive bus 270. Transmit cell FIFO (TCF) 240 may be utilized to communicate to either switch 80 or TCA 90 via SIB transmit bus 260. Further, the TCF 240 interfaces to two micro-engines referred to as DMA packet controller send queue (SQ) 210 and DMA packet controller receive queue (RQ) 220. The function of the TCF 240 is to assemble a packet using the header from the DMA packet controller ~~are queue~~ RQ 220 or SQ 210 and the payload data from the memory controller 50. The payload 920 portion (Figure 7) of the packet may be typically received from memory controller 50. In order for this and other functions to be performed, TCF 240 contains a buffer control logic 300 and a cell buffer byte alignment logic (BAL) 310. The buffer control logic 300 is discussed in further detail in reference to FIG. 3. The cell buffer BAL 310 is discussed in further detail in reference to FIG. 4.